ISSN: 2350-0328

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 4, Issue 6 , June 2017

High Speed Energy Efficient 16 Bit Carry Skip Adder

Mala.H.N, Dr.K.V.Prasad

MTech student, Department of ECE, Bangalore Institute of Technology, Bengaluru
Professor and HOD, Department of ECE, Bangalore Institute of Technology, Bengaluru

ABSTRACT: In this paper we have designed a 16 bit carry skip adder (CSKA) which has higher speed and energy efficient compared to the conventional carry skip adder (CSKA).The performance and efficiency of conventional carry skip adder structure is improved by employing increment and concatenation scheme. In the existing system the multiplier is used which consumes more power. Instead of using this structure that consists of AND-OR-INVERTER (AOI) and OR-AND-INVERTER (OAI) is used for skip logic. Further development in energy and speed can be achieved by the structures with both variable and fixed stage size. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. To achieve this we are using Xilinx ISE and Modelsim simulator. The proposed structures are assessed by comparing their Device utilization summary and power. By this project we can able to compare the adders performance and results.

KEYWORDS: compound gates, AND-OR-INVERT,OR-AND-INVERT, majority gate, carry skip adder, incrementation block, energy efficient, fixed stage size, x power analyser, design summary, etc…

I.INTRODUCTION

An **adder** is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures along with their characteristics may be found in [1] and [4]. TheRCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA. The PPAs, which are also called carry look-ahead adders, exploit direct parallel prefix structures to generate the carry as fast as possible.

In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic. The concentration on the static CMOS originates from the desire to have a reliably operating circuit under a wide range of supply voltages in highly scaled technologies. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the superthreshold region down to near-threshold region and also, the design of (hybrid) variable latency CSKA structures have been reported in the literature. Hence, the contributions of this paper can be summarized as follows.

1) Proposing a modified CSKA structure by combining the concatenation and the incrementation schemes to the conventional CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer.

2) Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay.

ISSN: 2350-0328

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 4, Issue 6 , June 2017

3) Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with an 8 bit adder designed with majority gate, which is modified in this paper

Conventional carry skip adder (CSKA)

The structure of an *N*-bit Conv-CSKA, which is based on blocks of the RCA (RCA blocks), is shown in Fig. 1. In addition to the chain of FAs in each stage, there is a carry skip logic. For an RCA that contains *N* cascaded FAs, the worst propagation delay of the summation of two *N*-bit numbers, *A* and *B*, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where
$Pi = Ai \oplus Bi = 1$ for $i = 1, \ldots, N$
where *Pi* is the propagation signal related to *Ai* and *Bi*. This shows that the delay of the RCA is linearly related to *N* [1]. In the case, where a group of cascaded FAs are in the propagate
mode, the carry output of the chain is equal to the carry input. In the CSKA, the carry skip logic detects this situation, and makes the carry ready for the next stage without waiting for the operation of the FA chain to be completed. The skip operation is performed using the gates and the multiplexer shown in the figure. Based on this explanation, the *N* FAs of the CSKA are grouped in *Q* stages. Each stage contains an RCA block with *Mj* FAs ($j = 1, \ldots, Q$) and a skip logic. In each stage, the inputs of the multiplexer (skip logic) are the carry input of the stage and the carry output of its RCA block (FA chain). In addition, the product of the propagation signals (*P*) of the stage is used as the selector signal of the multiplexer[5].

Here, the stage size is the same as the RCA block size. In addition to the chain of FAs in each stage, there is a carry skip logic. For an RCA that contains *N* cascaded FAs, the worst propagation delay of the summation of two *N*-bit numbers, *A* and *B*, belongs to the case where all the FAs are in the propagation mode.

It means that the worst case delay belongs to the case where

$$P_i = A_i \oplus B_i = 1 \text{ for i} = 1,\ldots,\text{N}$$

where *Pi* is the propagation signal related to *Ai* and *Bi*. This shows that the delay of the RCA is linearly related to *N*.
In the case, where a group of cascaded FAs are in the propagate mode, the carry output of the chain is equal to the carry input. In the CSKA, the carry skip logic detects this situation, and makes the carry ready for the next stage without waiting for the operation of the FA chain to be completed. The skip operation is performed using the gates and the multiplexer shown in the figure. Based on this explanation, the *N* FAs of the CSKA are grouped in *Q* stages. Each stage contains an RCA block with *Mj* FAs ($j = 1, \ldots, Q$) and a skip logic. In each stage, the inputs of the multiplexer (skip logic) are the carry input of the stage and the carry output of its RCA block (FA chain). In addition, the product of the propagation signals (*P*) of the stage is used as the selector signal of the multiplexer.

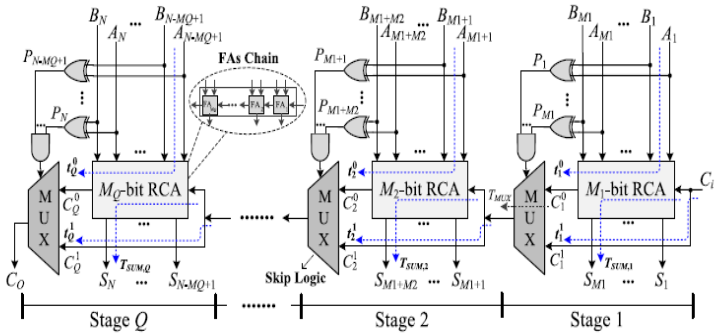

Fig1: conventional carry skip adder

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder. Many methods have been suggested for finding the optimum number of the FAs. In, some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause

ISSN: 2350-0328
International Journal of Advanced Research in Science, Engineering and Technology
Vol. 4, Issue 6 , June 2017

area and power increase considerably and less regular layout. The design of a static CMOS CSKA where the stages of the CSKA have a variable sizes was suggested in [18]. In addition, to lower the propagation delay of the adder, in each stage, the carry look-ahead logics were utilized. Again, it had a complex layout as well as large power consumption and area usage.

II. SIGNIFICANCE OF THE SYSTEM

The existing CSKA has more delay and power consumption and some of the proposed methodologies uses some complex methodologies to achieve less delay and low power consumption. The design of conventional carry skip adder, modified carry skip adder and the proposed carry skip adder of 16 bit are done using Xilinx ISE and simulated on modelsim simulator and we are not using any high level complex simulation tools. Xilinx officially supports Microsoft Windows, Red Hat Enterprise 4, 5, & 6 and many other operating systems and it is freely available not necessary to get the licence for the usage.

In this paper what we are proposing for Reduction of power and delay is the simple method just through the modification in the structure of an adder, without applying any high level algorithms and methodologies. We are modifying the structure of the conventional CSKA in two stages. In the first stage we makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic instead of utilizing multiplexer logic. This will reduces the critical path delay considerably but not the power as expected. Hence in the second stage we are designing an 8 bit adder using majority gate and replacing the middle 8 bit RCA blocks with the designed one. By this modification to the first stage modification we are getting less delay and less power consumption compared to the previous designs.

III. LITERATURE SURVEY

.
From past 10 years there are many methodologies or techniques are developed to optimize the performance parameters like power and speed. In terms of reducing the delay we are increasing the speed and we are reducing the power by reducing both area and delay.
Karthik.D proposed a technique in which they are modifying the structure of the conventional carry skip adder and they are replacing the intermediate stages of the adder with parallel prefix adder (PPA). This method we are following in this paper but instead of PPA we are developing an 8 bit majority gate based adder. And we are using Xilinx ISE tool and Modelsim simulator.

. K Vijaya Krishna proposed a adder which works on majority gate based logic reduction technique by using quantum cellular automata which is a nanotechnology based technique. In this we are taking the logic or working of the majority gate and we are developing that majority gate using the VHDL coding technique instead of nanotechnology

K. Chirca *et al.* proposed a high speed 32 bit carry skip adder which is based on static CMOS technology. Which is based on subthreshold region of working of the transistor. But it is complex one and mainly based on transistor level design.

H. M. Kittur propsed a design for high speed carry select adder, which is also based on static CMOS design. They are modifying the carry select logic and hence the structure of the adder.

Mainly in almost all methods they are modifying the skip logic and intervensioning of the designed adder. We are also using these formats with different, simple and efficient methodologies.

ISSN: 2350-0328

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 4, Issue 6 , June 2017

IV. METHODOLOGY

The structure is based on combining the concatenation and the incrementation schemes [13] with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates (Fig. 2). The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated. As shown in Fig2, if an AOI is used as the skip logic, the next skip logic should use OAI gate. In addition, another point to mention is that the use of the proposed skipping structure in the Conv-CSKA structure increases the delay of the critical path considerably.

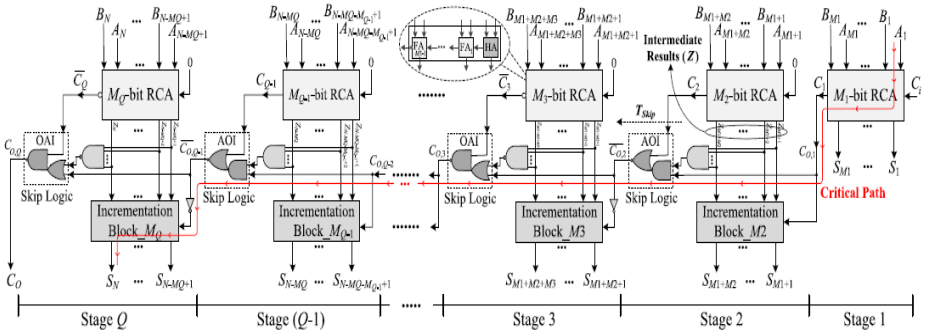

Fig 2. Proposed structure of CSKA

This originates from the fact that, in the Conv-CSKA, the skip logic (AOI or OAI compound gates) is not able to bypass the zero carry input until the zero carry input propagates from the corresponding RCA block. To solve this problem, in the proposed structure, we have used an RCA block with a carry input of zero (using the concatenation approach). This way, since the RCA block of the stage does not need to wait for the carry output of the As mentioned before, the use of the static AOI and OAI gates (six transistors) compared with the static 2:1 multiplexer (12 transistors), leads to decreases in the area usage and delay of the skip logic. In addition, except for the first RCA block, the carry input for all other blocks is zero, and hence, for these blocks, the first adder cell in the RCA chain is a HA. This means that $(Q - 1)$ FAs in the conventional structure are replaced with the same number of HAs in the suggested structure decreasing the area usage.

In addition, note that the proposed structure utilizes incrementation blocks that do not exist in the conventional one. These parts include the chain of the FAs of the first stage, the path of the skip logics, and the incrementation block in the last stage. The delay of this path (*TD)* may be expressed as

$$T_D = [M_1 T_{\text{CARRY}}] + \left[(Q-2)\left(\frac{T_{\text{AOI}} + T_{\text{OAI}}}{2}\right)\right] + [(M_Q - 1)T_{\text{AND}} + T_{\text{XOR}}]$$

Fixed stage size technique

By assuming that each stage of the CSKA contains *M* FAs, there are $Q = N/M$ stages where for the sake of simplicity, we assume Q is an integer. The input signals of the j th multiplexer are the carry output of the FAs chain in the j th

ISSN: 2350-0328
International Journal of Advanced Research in Science, Engineering and Technology
Vol. 4, Issue 6 , June 2017

stage denoted by *C*0*j*, the carry output of the previous stage (carry input of the *j* th stage) denoted by *C*1*j* (Fig. 1). The critical path of the CSKA contains three parts:
1) the path of the FA chain of the first stage whose delay is equal to $M \times T\text{CARRY}$
2) the path of the intermediate carry skip multiplexer whose delay is equal to the $(Q-1)\times T\text{MUX}$
3) the path of the FA chain in the last stage whose its delay is equal to the $(M-1) \times T\text{CARRY} + T\text{SUM}$. Note that *T*CARRY, *T*SUM, and *T*MUX are the propagation delays of the carry output of an FA, the sum output of an FA, and the output delay of a2:1 multiplexer, respectively. Hence, the critical path delay of a FSS CSKA is formula

$$T_D = [M \times T_{\text{CARRY}}] + \left[\left(\frac{N}{M} - 1\right) \times T_{\text{MUX}}\right] + [(M-1) \times T_{\text{CARRY}} + T_{\text{SUM}}]. \quad (1)$$

Modification in the proposed CSKA

We are modifying the proposed structure to achieve low power consumption and to get the lower delay compared to the previous one. By this design we are optimizing the parameters like power and delay.to do this we are designing an 8 bit adder which is based on majority gate. the majority gate is like a basic gate in quantum cellular automata(QCA) technique. We are not using this nano scale technique instead we are taking the logic of that majority gate. By using the normal basic gates like AND gate, OR gate etc., we are designing an 8 bit adder. Majority gate is the one its output will be one if the majority of the inputs are one. This 8 bit adder replaces the intermediate stage of the 16 bit carry skip adder.

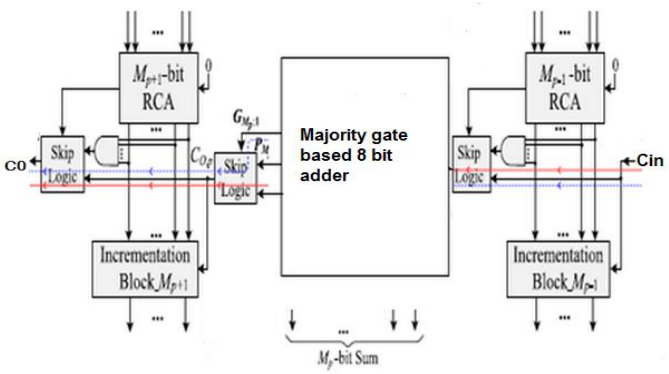

Fig 3: modified Proposed CSKA

V. EXPERIMENTAL RESULTS

The design of conventional carry skip adder, modified carry skip adder and the proposed high speed energy efficient carry skip adder of 16 bit are done using Xilinx ISE and simulated on modelsim simulator and Delay and power consumption of those adders are tabulated..

ISSN: 2350-0328
International Journal of Advanced Research in Science, Engineering and Technology
Vol. 4, Issue 6 , June 2017

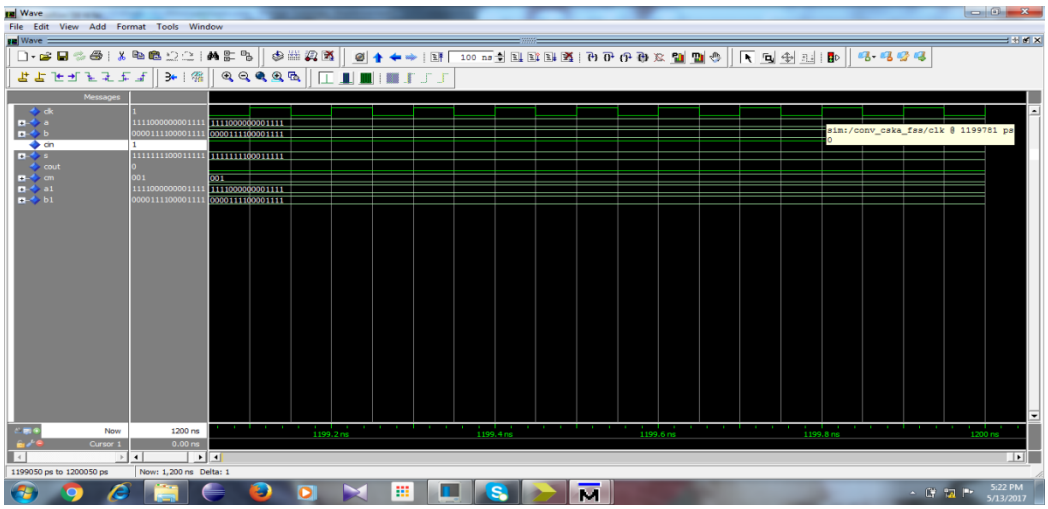

Fig 5: Simulation output of the high speed energy efficient 16 bit CSKA

Fig5, Fig6 and fig7 shows the simulated output and the information about the delay in the design summary and the power consumption in the X power analyzer window respectively

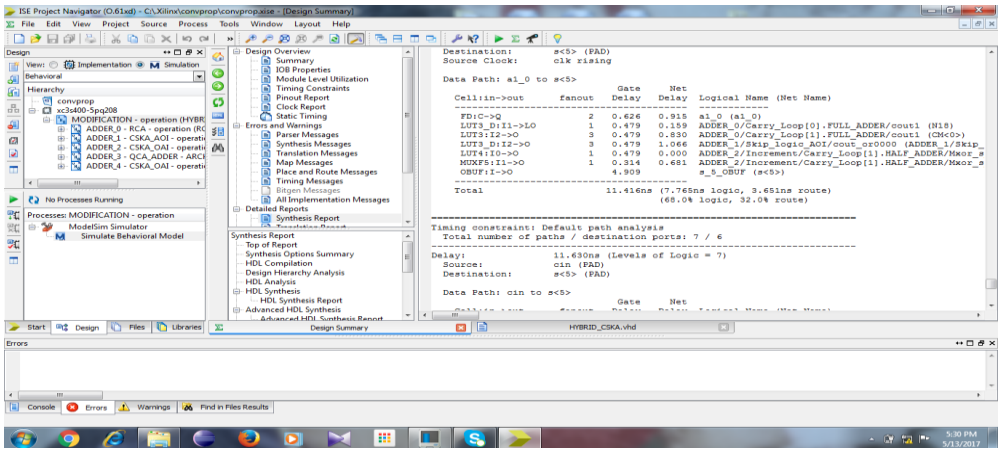

Fig 6: Delay output of the high speed energy efficient CSKA

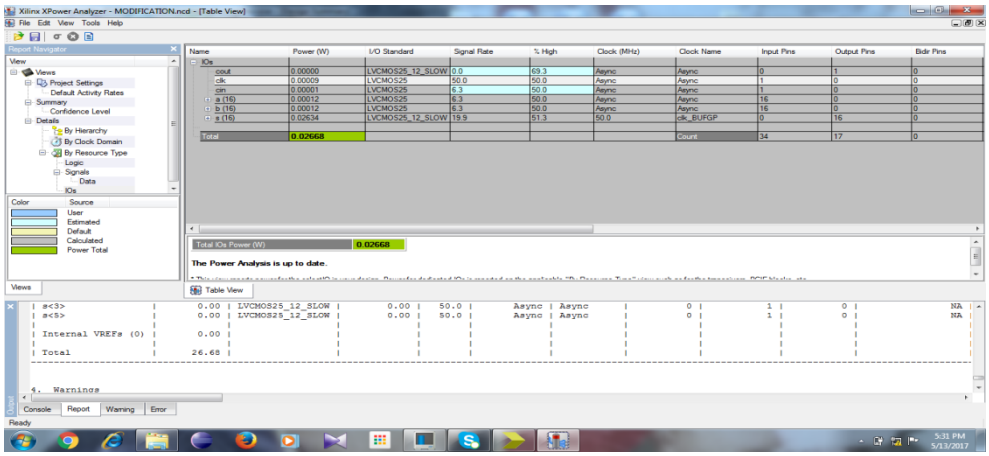

Fig 7: X power analyzer result of high speed energy efficient 16 bit CSKA

ISSN: 2350-0328
International Journal of Advanced Research in Science, Engineering and Technology
Vol. 4, Issue 6 , June 2017

Adder	Delay	Power
Existing CSKA	35.53nS	35.95mW
Modified CSKA	17.34nS	31.5mW
Proposed CSKA	11.41nS	26.3Mw

Table 2: comparison of results

VI. CONCLUSION AND FUTURE WORK

The proposed carry skip adder has less delay and lower power consumption compared to the conventional CSKA. The proposed structure reduces the delay considerably. In ordered to achieve both the parameters like lower power and less delay we are modifying the proposed one. Delay reducing means that we are achieving higher speed. Hence it has the name high speed and energy efficient CSKA. We can compare the results with some other previous designs.

.

REFERENCES

1. Karthik.D, Jayamani.S "High speed energy efficient carry skip adder operating at different voltage supply" accepted to be presented at the IEEE WiSPNET 2016 conference
2. Milad Bahadori, Mehdi Kamal, Ali Afzali-Kusha, *Senior Member, IEEE*, and Massoud Pedram, *Fellow, IEEE* "High speed energy efficient carry skip adder operating at different voltage supply" 2015
3. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no.2, pp. 371–375, Feb. 2012
4. Y. He and C.-H. Chang, "A power-delay efficient hybrid carrylookahead/carry-select based redundant binary to two's complement converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 1, pp. 336– 346, Feb. 2008
5. K.Vijaya Krishna1, R.Radha Krishna2 "Design of the Best Area-delay Adders with QCA Majority Logic Gates by using VHDL" International Journal of Scientific Research Engineering & Technology (IJSRET), ISSN 2278 – 0882 Volume 4, Issue 10, November 2015
6. K. Chirca *et al.*, "A static low-power, high-performance 32-bit carry skip adder," in *Proc. Euromicro Symp. Digit. Syst. Design (DSD)*, Aug./Sep. 2004, pp. 615–619.
7. S. Jia *et al.*, "Static CMOS implementation of logarithmic skip adder," in *Proc. IEEE Conf. Electron Devices Solid-State Circuits*, Dec. 2003, pp. 509–512.
8. M. Alioto and G. Palumbo, "A simple strategy for optimized design of one-level carry-skip adders," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 1, pp. 141–148, Jan. 2003